M.S. THESIS

Analysis of leakage current according to the impact of bulk traps in strained n-FinFETs

벌크 트랩이 strained n-FinFETs의 누설전류에 미치는 영향 분석

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ABSTRACT

A strained n-type FinFET which uses SiGe buffer layer for tensile stress is designed based on CMOS technology. This device generates bulk traps because of the lattice mismatch between SiGe layer and silicon layer. This structure is simulated in order to investigate the impact of bulk trap on the leakage current.

It is observed that the leakage current is generated mainly in the region of top of the Fin because electric field is concentrated. For specification, Fin is divided in to four portions according to the Fin height. It is observed that the leakage current is generated 42%, 29%, 26%, and 3% from top to bottom.

The impact of bulk-traps is analyzed by simulation. It is assumed that the bulk-traps are acceptor like trap which is distributed uniformly. The bulk traps are located in the spacer region which is important in analyzing leakage current. The numbers of bulk traps in each region are assumed to be identical for

comparison. The simulation results show that the leakage current decreases when the bulk traps exist. The decrease rate decreases from top to bottom and there is marginal difference in the bottom region of the Fin. When the traps capture the electrons, an energy barrier is formed resulting in increase of the tunneling distance. Also, the peak electrical field decrease because of the traps.

Keywords : Leakage current, FinFETs, 3-D Simulation, Traps. Band to band tunneling

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CONTENTS

1. Introduction

As CMOS technology has been developed, enhancing performance by scaling has become a challenging issue in recent days. Strain engineering has become an alternative method for enhancing CMOS performance by reducing effective mass. Usually, n-type Field Effect Transistor (FET) reduces mass by tensile stress, while p-type FET uses compressive stress [1-3]. In this study, we focused on strained n-type FET.

Off-state leakage is one of the major issues to be considered in reliability and performance characteristics of CMOS devices [4-5]. It is also important to consider off-state leakage current in strained devices. Strained FET generates traps in the inside of the device. This is due to the fact that lattice mismatch occurs in the interface between $Si_{1-x}Ge_x$ layer, which produce strain, and silicon layer, which is a channel region. Lattice mismatch generates bulk traps instead of interface traps. Even though, there are numerous studies of interface traps [6-8], there are currently rare studies on the impact of the bulk traps. In this work, the critical effect of a bulk traps are studied in detail.

FinFET is developed with special emphasis on process simplicity

and compatibility with conventional planar CMOS technology [9]. In order to follow this trend, we focused on n-type strained FinFET and performed simulation of the impact of bulk traps. FinFET shows the different mechanism of leakage current compared to planar bulk MOSFET [10]. In the case of FinFET, most of the leakage current generates through the spacer region. Thus, the analysis of leakage current should be focused on specific region.

In n-type strained FinFET there are large off-leakage current due to smaller band gap [11] and many traps. At this point, traps mainly contribute to trap-assisted tunneling (TAT) while band-to-band tunneling (BTBT) is attributed to small band gap. Generally, traps are considered in trap assisted tunneling mechanism [12] and ignored in band to band tunneling mechanism [13].

Large trap density, however, creates a buffer area in a channel bulk region. The buffer area relieves the energy band bending and decreases band to band tunneling current. If the device is operated in band to band tunneling regime at V_{DD}, the traps could suppress off-leakage current in a region where the main band to band tunneling current is generated. In this paper, we analyzed the decrease of band to band tunneling current depending on trap density. There were comprehensive understandings for the impact

of traps on band to band tunneling region as buffer.

2. Simulation Setup

A TCAD process tool, Senaturus [14], comprising of process and device simulation capabilities is used for this paper. Figure 1 shows the device structure in three dimension simulation structure and cross section of strained n-FinFET.

The gate length is 150nm to suppress the short channel effect. The channel region is separated to assign the different trap density in this work. Fin height is set as 40nm in order to analyze the leakage current according to the height. The fin is divided into four parts (each by 10nm) to analyze the impact of bulk traps. The buffer layer, which induce strain, is consists of 0.3 of germanium and 0.7 of silicon ($Si_{0.7}Ge_{0.3}$). The overlap region of the device is 1.8nm and the doping of source and drain is $1x10^{20}cm^{-3.}$

To run the TCAD simulation, following models are included and activated: band gap narrowing model, Shockley-Read-Hall(SRH) recombination model, Hurkx TAT & BTBT model[12,13,15], doping dependent mobility degradation model, high field saturation mobility model in which carrier drift velocity is no longer proportional to the electric field in high field region, and electron' s normal mobility model which is used as mobility degradation at interfaces. Moreover,

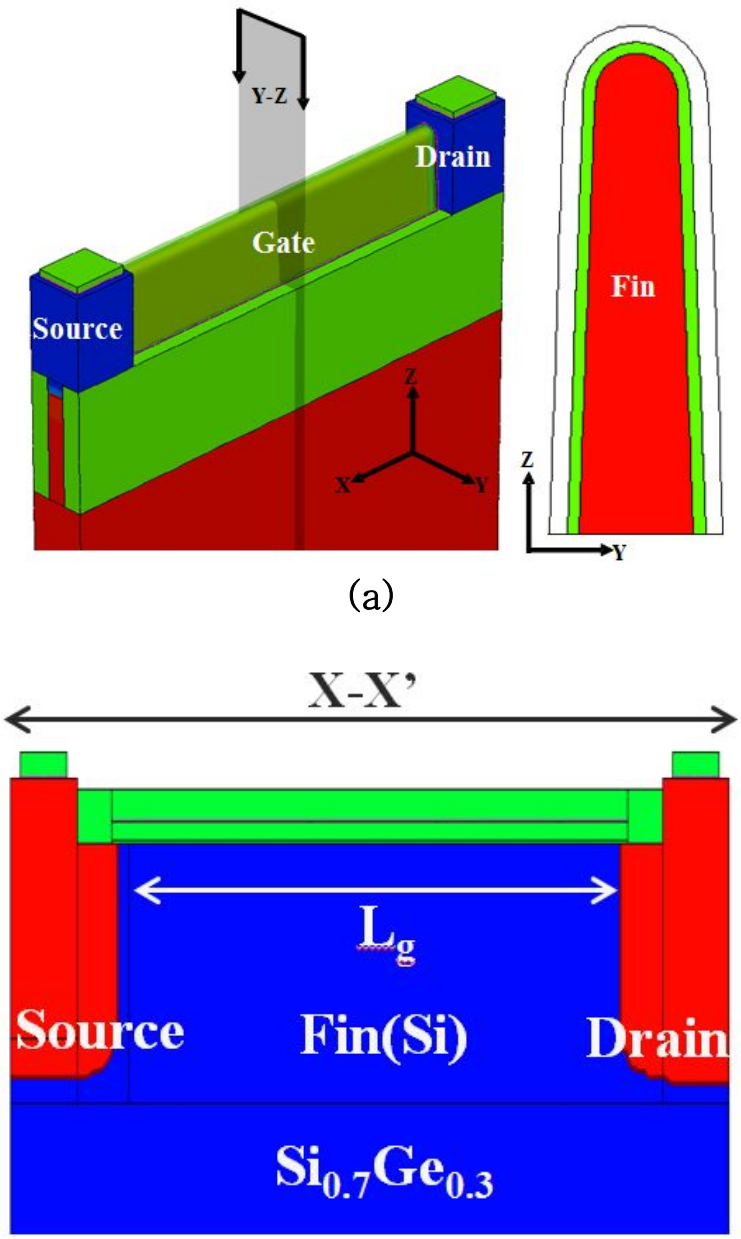


Fig. 1. (a) Three-dimensional bird's s-eye view of n-type FinFET. (b) Cross-sectional view of FinFET along the channel.

the Fermi Dirac statistics [14] are applied to all the simulations.

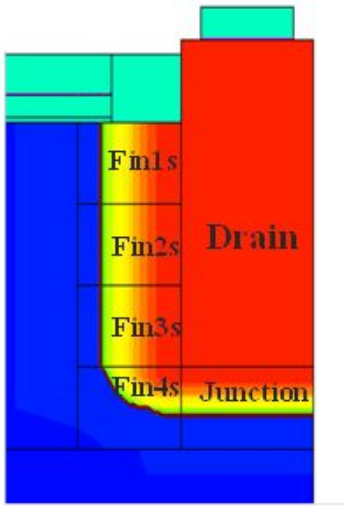
It is reported that the leakage current is generated mainly because of traps [16]. As bulk traps are generated in the interface of SiGe and silicon, it is important to study the impact of traps. The impact of traps is studied in the worst case that maximizes the impact of traps on the leakage current. As FinFET is susceptible to traps located at the spacer region [6], it is assumed that the traps are located at the spacer region randomly. Also, the characteristics of traps are assumed to be acceptor like and charge neutral level (CNL) in energy mid-gap. The capture cross section is $1x10^{-12}cm^{-2}$. As the traps differently affect the leakage current according to its location, spacer near the drain region is separated into four parts. Each of the parts is separated in same Fin height (10nm) but it has different volume. Each region is designate as Fin1s, Fin2s, Fin3s, and Fin4s+Junction from top to bottom. The Fin4s+Junction place includes the bottom of the Fin and the junction between drain and substrate. To study the impacts of trap, according to its location, 50 traps are located in only one region, while other region does not contain traps.

3. Results

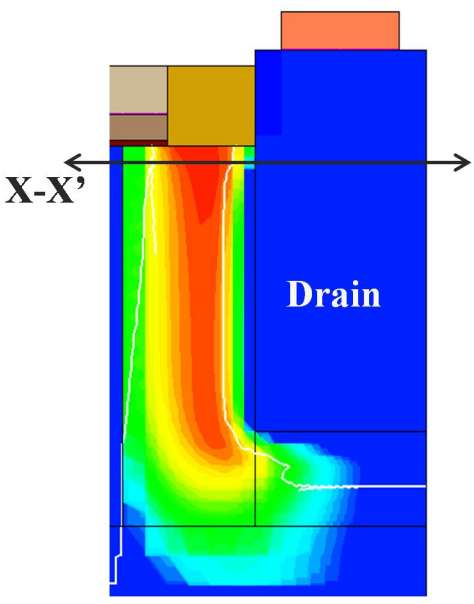
Figure 2 (a) and (b) shows the simulation results of the device structure. The doping profile (Fig 2.1 (a)) gradient is 11.6nm and the spacer is divided correctly. It shows that band to band tunneling, main leakage current component, is concentrated on the top of the spacer when the drain voltage is 1.5V and gate is 0V. There is relatively less band to band tunneling current at the bottom of the Fin.

Figure 3 shows the leakage current per width according to the traps location. In the low field region (V_{DG} < 0.6V), subthreshold leakage is the main leakage current. The subthreshold leakage current is not significantly affected by traps. In the high field region(V_{DG} > 0.6V) the leakage current is constitute of band to band tunneling current. Generally, the simulation results show that the leakage current decreases when traps exist. However, the decrease rate depends on the trap location. When traps are located in Fin1s, the leakage current decreases significantly. On the other hand, leakage current decrease rate diminishes when traps are located in Fin2s, Fin3s, and the bottom region. Especially when traps are

located in Fin4s+Junction region, the leakage current decreases rate is marginal.

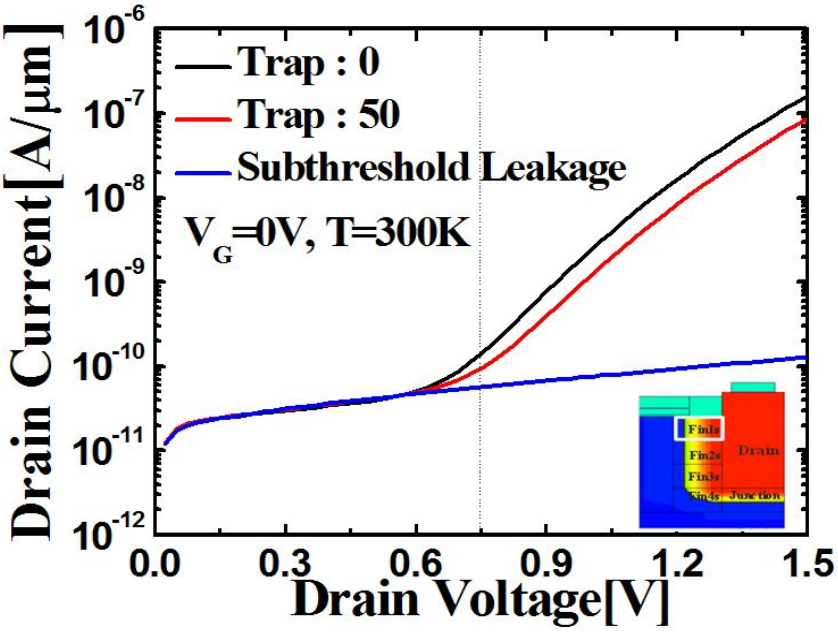


(a)

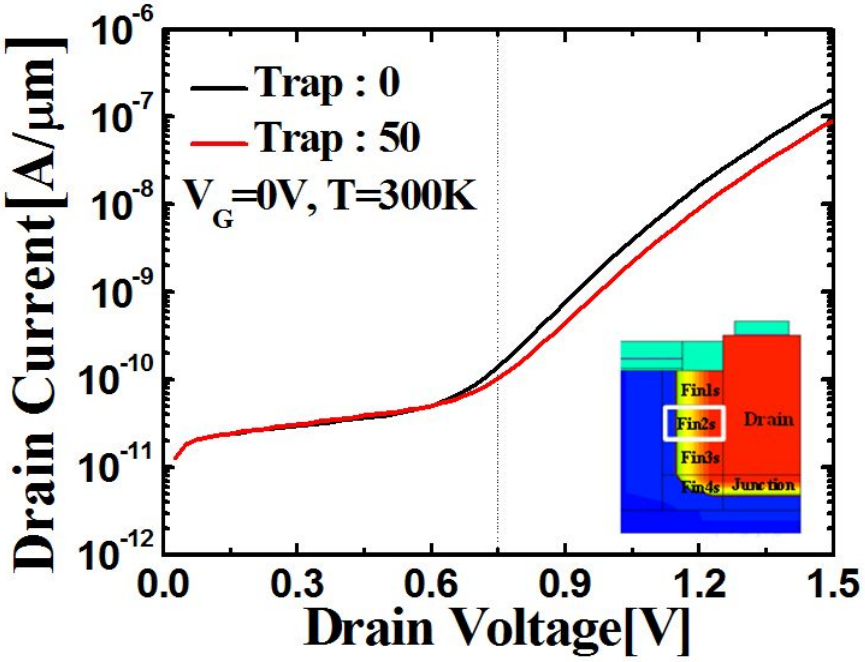


(b)

Fig. 2. (a) Fin split and the doping profile. (b) Band to band tunneling concentration in the spacer region(V_D=1.5V,V_G=0V).

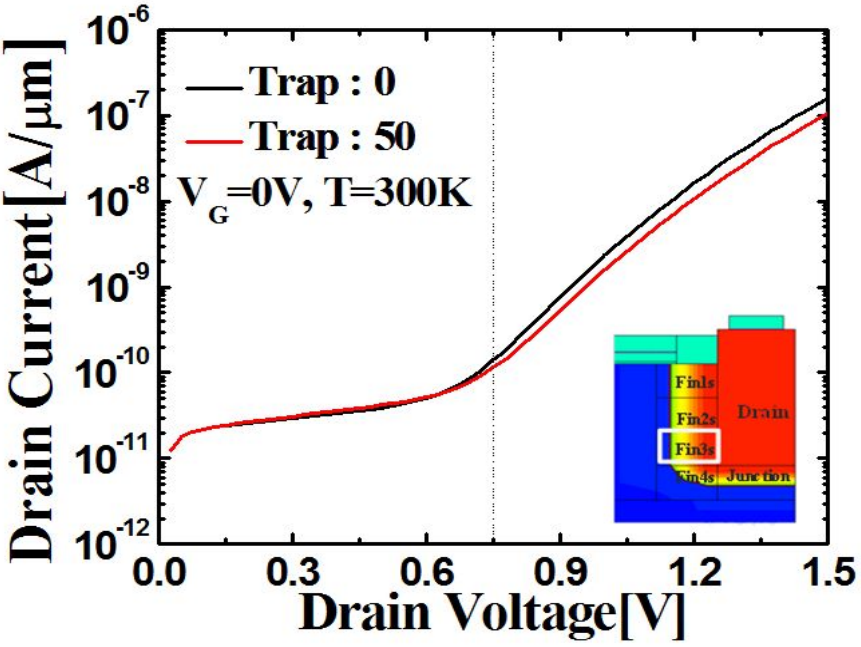


(a)

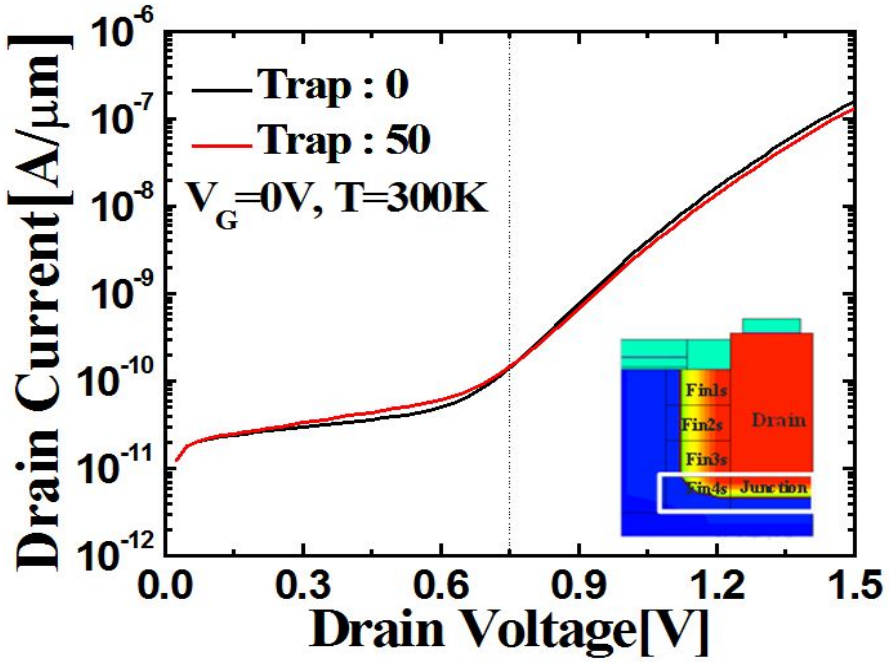


(b)

Fig. 3. 1. Simulation results of leakage current at different trap position. ((a) Fin1s, (b) Fin2s, (c) Fin3s, and (d) Fin4s+Junction)



(c)



(d)

Fig. 3. 2. Simulation results of leakage current at different trap position. ((a) Fin1s, (b) Fin2s, (c) Fin3s, and (d) Fin4s+Junction)

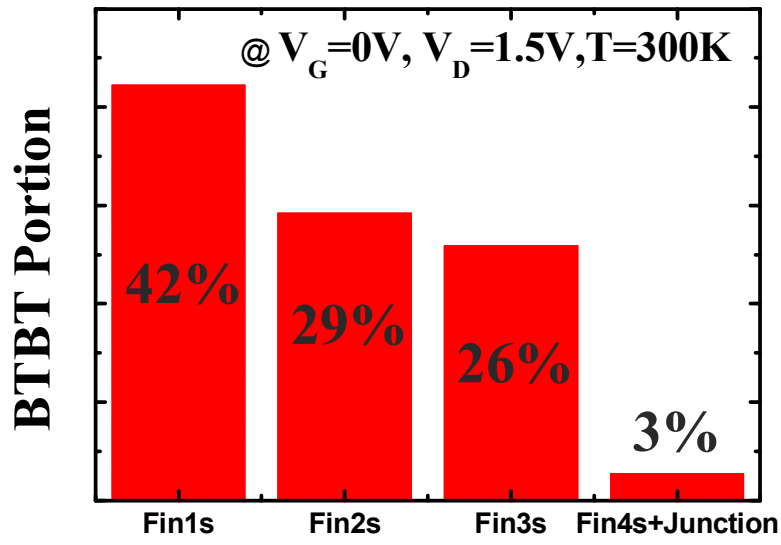
4. Discussion

The leakage current of strained n-FinFET at low field is generated universally in the as shown in figure 3.1 (a). The main leakage current is mainly consisted of subthreshold leakage current. In this simulation the trap assisted tunneling (TAT) current is smaller than the subthreshold leakage current because of weak substrate doping. However, trap assisted tunneling current increases because of traps. This is attributed to the fact that additional traps generate supplementary path for trap assisted tunneling current. Trap assisted tunneling increase proportionally to the number of traps. If the subthreshold leakage current is reduced through body doping, and longer gate channel the main leakage current would be consisted of trap assisted tunneling. If the trap assisted tunneling is the main leakage current, it would be affected by the number of traps resulting in increase of total leakage current.

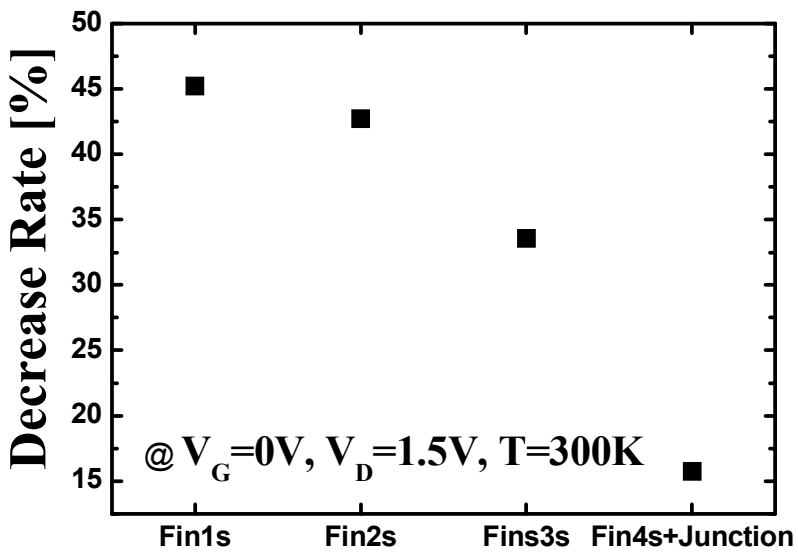
The leakage current of strained n-FinFET at high field is generated usually in the top of the fin as shown in figure 2. Specifically, most of the band to band tunneling current is generated in the region through Fin1s to Fin3s. Figure 4 (a) shows the portion of band to band tunneling current. Fin1s generates 42% of the

leakage current which is the largest portion. Fin2s and Fin3s generates similar portion of leakage current which is 29% and 26% respectively. The bottom region, Fin4s+Junction, generates marginal leakage current which is 3%. The different portion is contributed to the fact that the field is stronger than the upper region because the contact is in the top of the drain region. Moreover, as the width of the Fin is smaller and the top of the fin is round shaped, fringing effect occurs resulting in high electric field. It is certain that band to band tunneling current is important, since the voltage difference between drain and gate is usually big in operation voltage. Thus, it is necessary to focus on band to band tunneling current.

Figure 4 (b) shows the decrease rate of band to band tunneling if traps exist. For comparison, we assumed that traps exist at only certain region (ex Fin1s), while the other regions (Fin2s, Fin3s, and Fin4s+Junction) have no trap. In the graph, the x-axis represents where traps exist. The band to band current decrease rate diminishes from the top of the fin to bottom. Specifically, from Fin1s to Fin4s+Junction, band to band tunneling current decrease rate is 45%, 43%, 35% and 16% respectively. Fin1s and Fin2s has similar decrease rate and Fin3s decrease rate is slightly smaller and the bottom of the Fin has very low decrease rate. This is because



(a)

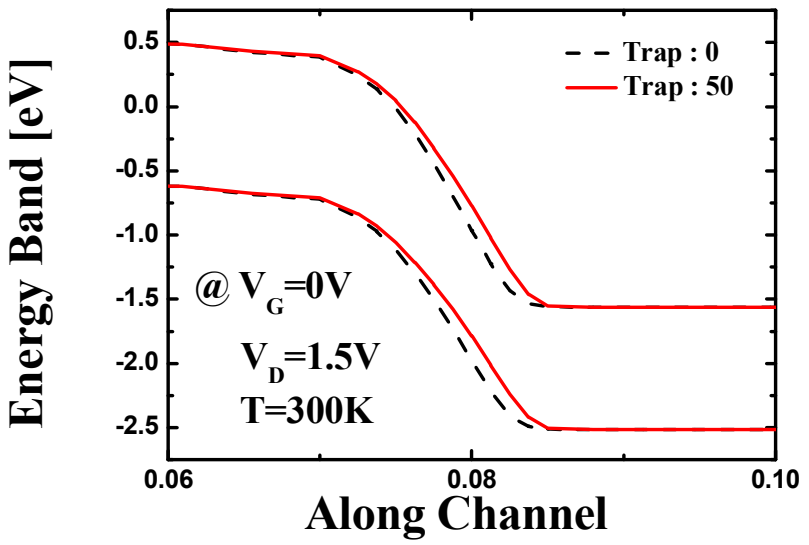


(b)

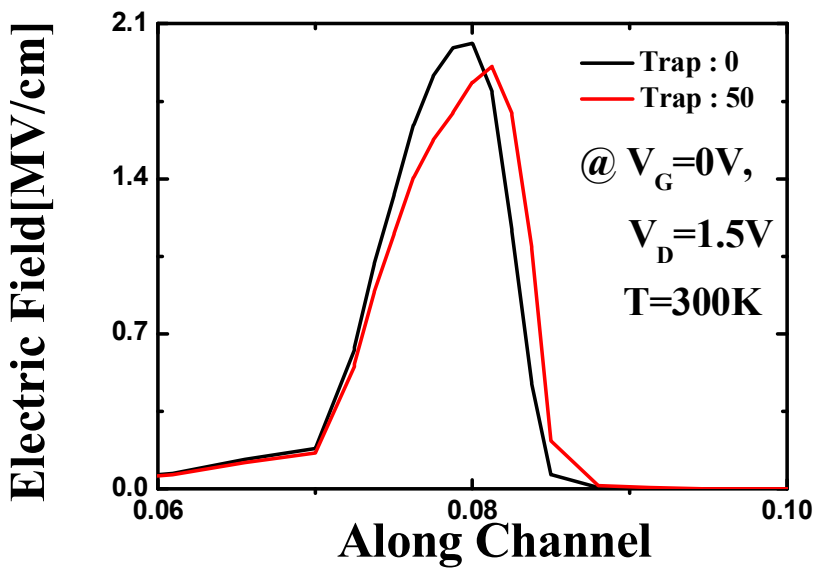
Fig. 4. (a) Leakage current (Band to band tunneling) portion and (b) decrease rate according to trap location.

the impact of the bulk traps is higher in the upper region. As the upper region has higher electrical field resulting in a large portion of leakage current, the impact of traps is larger when traps are located. On the other hand, the bottom of the Fin has low electric field which means the impact of the traps is marginal.

Figure 5 (a) shows the energy band diagram and (b) shows the electric field of strained n-FinFET based on simulation. Gate voltage is set as 0V and drain voltage is set as 1.5V at 300K. It is the region of gate overlap through spacer and drain at 37.5nm of Fin height (Fin1s region). The left part is the gate overlap region (60nm ~ 70nm) and the middle part represents the spacer region (70nm ~ 85nm). The right part is drain region (85nm~). The dashed line represents the energy band diagram with no traps. The solid line represents the energy band diagram when 50 traps are located in the spacer region. It shows that energy band diagram slop has decreased when traps exist. As a result, the tunneling path has increased resulting in leakage current decrease. This is because when electrons are trapped inside the traps, additional energy barrier is formed. Trapped electrons transiently increase the energy band at that point and additional energy barrier is formed. Thus, this additional energy barrier prevents electrons in valance band from tunneling to the conduction band. The total number of el-



(a)



(b)

Fig. 5. (a) Energy band diagram and (b) electric field comparison between no trap and 50 trap in Fin1s region. (V_G=0V, V_D=1.5V, and Fin height 37.5nm)

ectrons that tunneling from valance band to conduction band decrease. The mechanism of tunneling electrons dominantly occurs where the tunneling path is the smallest. Traps change the energy band diagram and the minimum tunneling length also changes as seen in Fig 5 (a).

Figure 5 (b) shows the electric field in the same condition as Fig 5 (a). The left solid line indicates the electric field when trap does not exist. The right solid line represents the electric field when traps are filled in Fin1s. The peak value of electric field has decreased when traps exist. The decrease rate of electric field is 20%. Electric field decreases because electrons are likely to be trapped and change the electric field. The band to band tunneling current is exponentially related according to the Hurkx model [12]. Thus, the leakage current decreases significantly. Also, the point where the electric field is peak has shifted. This is the place where band to band tunneling process mainly occurs. The point has shifted approximately 10nm. The shift of the peak electric point is due to the fact that the trapped electrons generates additional energy

barrier resulting in a change of position where the tunneling process occurs.

5. Conclusion

The leakage current characteristics were studied for strained n-FinFET. The leakage current is generated mostly in the top of the Fin because the electric field is concentrated. Traps are generated in the interface between SiGe layer and silicon because of lattice mismatch. The traps are generated toward the top through the mismatch region. As the traps exist in the spacer region, the trap assisted tunneling leakage current increases. However, the band to band tunneling leakage current decreases. This is because the traps play a significant role in diminishing the band bending. This changes the tunneling path and change of electric field. The traps could suppress off-leakage for certain operation voltages.

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초 록

SiGe 층을 이용한 tensile stress를 이용해 더 나은 효율을 가지는 n형 FinFET을 CMOS 기술을 바탕으로 디자인하였다. Tensile stress를 주는 SiGe층과 실제로 채널 생성되는 곳의 물질이 다르기 때문에 격자 상수 불일치가 발생하게 된다. 격자 상수 불일치는 내부에 빈자리가 생기거나 멀어진 거리로 인해 dangling bond가 생성이 되어 소자 내부에 벌크 트랩을 생성하게 된다. 벌크 트랩이 이 소자의 누설전류에 끼치는 영향을 시뮬레이션을 통해 연구하였다. 우선, 누설전류의 특성을 보기 위해 벌크 트랩이 없는 상태의 FinFET을 시뮬레이션하여 확인하였다. FinFET의 경우 전계가 Fin의 윗 부분에 집중되기 때문에 많은 부분의 누설전류가 생성이 되는 것을 확인하였다. 자세히 알기 위해 Fin을 위에서부터 네 등분하여 누설 전류의 비율을 확인하였다. Fin의 가장 높은 곳이 전체 누설 전류의 42%를, 그 다음 두 번째

위치에서 29%를 그리고 세 번째 영역에서 26% 마지막 바닥 부분에서 3%에 해당하는 비율로 누설전류를 생성하는 결과를 보였다.

각 영역에 대해서 벌크 트랩이 발생시키는 전류 변화를 시뮬레이션으로 확인하였다. 스페이서 영역에 존재하는 트랩의 영향이 크기 때문에, 스페이서 영역에 벌크 트랩을 위치시켰다. 트랩의 종류는 acceptor type으로 uniform 하게 분포한다고 가정하였다. Fin의 윗 세 영역은 벌크 트랩이 존재 할 때 누설 전류가 감소하며, 바닥 부분에서는 벌크 트랩이 누설전류에 영향을 거의 미치지 않는다는 것을 확인 하였다. 트랩이 존재할시 감소하는 전류 비율은 윗부분이 가장 컸으며, 바닥 부분으로 갈 수록 감소 비율은 감소하였다. 전류가 감소하는 경향을 분석하기 위해 에너지 밴다이어 그램, 전계를 분석 하였다. 벌크 트랩이 스페이서 영역에 존재 할 때, 전자가 트랩에 잡히게 되면 energy barrier를 형성하게 된다. 추가적인 energy barrier는 터널링 거리를 늘어나게하기 때문에 누설전류에 감소를 야기한다. 또한, 최대 전계 또한 감소하기 때문에 누설전류가 감소하게 된다.

주요어 : Strained n-FinFETs, Leakage current, Bulk trap, 3-D TCAD simulation.

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